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NIXON & VANDERHYE, PC
901 NORTH GLEBE ROAD, 11TH FLOOR
ARLINGTON, VA 22203

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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte DAVID JOHN BUTCHER, HEDLEY JAMES FRANCIS, STEPHEN JOHN HILL, VLADIMIR VASEKIN, and ANDREW CHRISTOPHER ROSE

Appeal 2009-005640[1]
Application 10/807,498[2]
Technology Center 2100

Decided: January 26, 2010

Before LEE E. BARRETT, JEAN R. HOMERE, and JAMES R. HUGHES, *Administrative Patent Judges*.

HUGHES, *Administrative Patent Judge*.

DECISION ON APPEAL

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[1] An oral hearing was held in this appeal on January 14, 2010.
[2] Application filed March 24, 2004. The real party in interest is ARM Limited. (App. Br. 1).

STATEMENT OF THE CASE

The Appellants appeal the Examiner's rejection of claims 1-60 under authority of 35 U.S.C. § 134(a). The Board of Patent Appeals and Interferences (BPAI) has jurisdiction under 35 U.S.C. § 6(b).

We reverse.

Appellants' Invention

Appellants invented a hardware decoder apparatus, as well as a method and computer program product for controlling the decoder. The decoder decodes program instructions that control processing logic so that the logic may perform data processing operations. The decoder, in response to a memory access instruction performs a null value check, i.e., compares a base register value with a predetermined null value. If a null value is detected, i.e., the base register value matches the predetermined null value, the decoder branches to a subroutine for handling the null value, i.e., a null value exception handler. (Spec. 2, ll. 10-23; 3, ll. 3-32.)[3]

[3] We refer to Appellants' Specification ("Spec."), Appeal Brief ("App. Br.") filed October 15, 2007, and Reply Brief ("Reply Br.") filed March 6, 2008. We also refer to the Examiner's Answer ("Ans.") mailed January 8, 2008.

Claim

Independent claim 1 further illustrates the invention. It reads as follows:

> 1. An apparatus for processing data comprising:
>
> processing logic operable to perform data processing operations; and
>
> an instruction decoder operable to decode program instructions to control said processing logic to perform data processing operations specified by said program instructions; wherein said instruction decoder, in response to a memory access instruction, compares a base register value, stored within a base register specified by a base register field of said memory access instruction, with a predetermined null value; and, if said base register value matches said predetermined null value, then said decoder triggers branching to execution of a null value exception handler.

Prior Art References

The Examiner relies on the following references as evidence of unpatentability:

Smith	US 5,430,862	Jul. 4, 1995
Mirapuri	US 5,590,294	Dec. 31, 1996
Click, Jr.	US 6,363,522 B1	Mar. 26, 2002

Andrew S. Tanenbaum, Structured Computer Organization 10-12 (2d ed. 1984).

Rejections on Appeal

The Examiner rejects claims 31-60 under 35 U.S.C. § 112, first paragraph as failing to comply with the enablement requirement.[4]

The Examiner rejects claims 31-60 under 35 U.S.C. § 112, second paragraph as being indefinite.[5]

The Examiner rejects claims 1, 6-11, 14-16, 21-26, 29-31, 36-41, 44-46, 51-56, 59, and 60 under 35 U.S.C. § 103(a) as obvious in view of Click and Smith.

The Examiner rejects claims 2-5, 12, 13, 17-20, 27, 28, 32-35, 42, 43, 47-50, 57, and 58 under 35 U.S.C. § 103(a) as obvious in view of Click, Smith, and Mirapuri.

ISSUE

Based on Appellants' contentions, as well as the findings and conclusions of the Examiner, the pivotal issue before us is as follows.

Did Appellants establish that the Examiner erred in finding the combination of the Click and Smith references collectively teaches an instruction decoder that, in response to a memory access instruction, compares a base register value, stored within a base register specified by a base register field of a memory access instruction, with a predetermined null value; and, if the base register value matches the predetermined null value, then the decoder triggers branching to execution of a null value exception handler as recited in claim 1?

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[4] The Examiner withdraws this rejection in view of Appellants' arguments. (Ans. 2, 17.) Therefore, we do not address the merits of this rejection.
[5] *See* footnote 4.

FINDINGS OF FACT (FF)

Click Reference

1. Click describes that processors (central processing units (CPUs)) and optimizers for converting a computer program are known in the art of computer hardware design and computer programming. (Col. 1, ll. 11-12, 22-23; col. 2, ll. 5-10.)

2. Click describes that it is known for a processor to perform null value checks for an invalid or null value pointer (col. 1, ll. 51-65; col. 2, ll. 5-15); and that "a test for a null pointer is implicitly performed when an attempt is made to load the contents associated with a pointer" (col. 1, ll. 63-65).

3. Click describes that it is known for an optimizer to handle exceptions associated with computer programs, including invalid pointer references, i.e., null value exception handling. (Col. 1, ll. 33-37, 41-43.)

4. Click describes that it is known to perform branching to execute a null value exception handler. (Col. 2, ll. 20-24.)

Smith Reference

5. Smith describes an emulator including a microprocessor and emulation chip (E chip) for decoding, translating, or converting computer instructions. Smith's microprocessor includes a register and an ALU. The E chip decodes each instruction and provides branch addresses to subroutines for executing the instructions. (Col. 2, l. 53 to col. 3, l. 1; col. 3, ll. 9-15; col. 4, ll. 40-43; Figs. 1, 2.)

PRINCIPLES OF LAW

Prima Facie Case of Unpatentability

The allocation of burden requires that the United States Patent and Trademark Office (USPTO) produce the factual basis for its rejection of an application under 35 U.S.C. § 103. *In re Piasecki*, 745 F.2d 1468, 1472 (Fed. Cir. 1984) (citing *In re Warner*, 379 F.2d 1011, 1016 (CCPA 1967)). The Examiner bears the initial burden of presenting a prima facie case of unpatentability. *In re Oetiker*, 977 F.2d 1443, 1445 (Fed. Cir. 1992). Appellants have the opportunity on appeal to the Board of Patent Appeals and Interferences (BPAI) to demonstrate error in the Examiner's position. *See In re Kahn*, 441 F.3d 977, 985-86 (Fed. Cir. 2006).

Obviousness

A claimed invention is not patentable if the subject matter of the claimed invention would have been obvious to a person having ordinary skill in the art. 35 U.S.C. § 103(a); *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007) (hereinafter "*KSR*"); *Graham v. John Deere Co.*, 383 U.S. 1, 13 (1966) (hereinafter "*Graham*"). The question of obviousness is resolved on the basis of underlying factual determinations including (1) the scope and content of the prior art, (2) any differences between the claimed subject matter and the prior art, (3) the level of skill in the art. *Graham*, 383 U.S. at 17-18. *See also KSR*, 550 U.S. at 407 ("While the sequence of these questions might be reordered in any particular case, the [Graham] factors continue to define the inquiry that controls.")

ANALYSIS

Click describes that null value checks and null value exception handling are known in the art. (FF 1-4.) Specifically, Click describes that processors and optimizers for converting computer programs are known, and that it is known for processors to perform null value checks. (FF 1, 2.) Click also describes that it is known for an optimizer to perform null value exception handling. (FF 3, 4.) Appellants admit that these mechanisms (null value checks and null value exception handlers) are "known within data processing systems." (Spec. 2, ll. 10-15.) Smith describes an emulator including a microprocessor and emulation chip (decoder) that decodes instruction and provides branch addresses to subroutines for executing the instructions. (FF 5.) We find that a skilled artisan would have understood the combination of the Click and Smith references to collectively teach processors, decoders, null value checks and null value exception handlers as recited in claim 1.

The Examiner contends that Click teaches a processor and a decoder (Ans. 17), as well as the claimed interaction between the processor and decoder – comparing a base register to a null value, and the decoder branching to a null value exception handler – but does not explicitly teach "[p]rocessing logic operable to perform data processing operations," or "[a]n instruction decoder operable to decode program instructions to control [the] processing logic to perform data processing operations specified by [the] program instructions" (Ans. 4). (*See* Ans. 3-4, 17-18.) Appellants, however, contend (*inter alia*) that the combination of the Click and Smith references does not teach "the claimed interrelationship between the 'processing logic' and the 'instruction decoder'" (App. Br. 11). (*See* App.

Br. 11-12, 16-17; Reply Br. 6.) Accordingly, we decide the question of whether the combination of the Click and Smith references collectively teaches an instruction decoder that, in response to a memory access instruction, compares a base register value, stored within a base register specified by a base register field of a memory access instruction, with a predetermined null value; and, if the base register value matches the predetermined null value, then the decoder triggers branching to execution of a null value exception handler.

After reviewing the record on appeal, we find the combination of the Click and Smith references does not teach an instruction decoder that performs a null value check and controls branching to a null value exception handler, i.e., in response to a memory access instruction, that compares a base register value, stored within a base register specified by a base register field of a memory access instruction, with a predetermined null value; and, if the base register value matches the predetermined null value, then the decoder triggers branching to execution of a null value exception handler. Rather, Click teaches that an optimizer is known to perform exception handling and a processor is known to perform null value checks. Smith teaches a processor and decoder, but is silent as to their interaction with respect to null values. (FF 1-5.) Neither reference describes, and the reference combination does not teach a decoder that performs both functions – performing a null value check and controlling branching to a null value exception handler. This limitation, in varying language and scope, is common to each of Appellants' independent claims 1, 16, 31, and 46.

For the foregoing reasons, Appellants have persuaded us of error in the Examiner's obviousness rejections of claims 1-60. Accordingly, we will not sustain the Examiner's rejections of these claims.

CONCLUSION OF LAW

On the record before us, we find that Appellants have established that the Examiner erred in finding the Click and Smith references collectively teaches an instruction decoder that, in response to a memory access instruction, compares a base register value, stored within a base register specified by a base register field of a memory access instruction, with a predetermined null value; and, if the base register value matches the predetermined null value, then the decoder triggers branching to execution of a null value exception handler.

DECISION

We reverse the Examiner's rejection of claims 1, 6-11, 14-16, 21-26, 29-31, 36-41, 44-46, 51-56, 59, and 60 under 35 U.S.C. § 103(a), and the Examiner's rejection of claims 2-5, 12, 13, 17-20, 27, 28, 32-35, 42, 43, 47-50, 57, and 58 under 35 U.S.C. § 103(a).

REVERSED

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Nixon & Vanderhye, PC
901 North Glebe Road, 11th Floor
Arlington, VA 22203